(1967 -)

Pallab Dasgupta

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AREAS OF EXPERTISE

Electronic Design Verification, Formal Methods, Artificial Intelligence

APPOINTMENTS

ACADEMIC APPOINTMENTS	2013-	Professor in Higher Administrative Grade, IIT Kharagpur
	2007- 2013	Professor, Dept. of Computer Science and Engineering, IIT Kharagpur
	2002- 2007	Associate Professor, Dept. of Computer Science and Engg, IIT Kharagpur
	1998- 2002	Assistant Professor, Dept. of Computer Science & Engg, IIT Kharagpur
	1995- 1998	Visiting Lecturer, I.I.T. Kharagpur
ADMINISTRATIVE APPOINTMENTS	2016- 2019	Dean, Sponsored Research and Industrial Consultancy, IIT Kharagpur
	2014- 2016	Associate Dean, Sponsored Research and Industrial Consultancy
	2009-	Director, Synopsys CAD Labs, IIT Kharagpur
	2007- 2010	Chairman, Advanced VLSI Consortium, IIT Kharagpur
	2019-	Professor-in-Charge, Academy of Classical and Folk Arts, IIT Kharagpur

AWARDS AND RECOGNITION

NATIONAL AWARDS

- Fellow of the Indian Academy of Science
- Fellow of the Indian National Academy of Engineering
- Young Scientist Medal of Indian National Science Academy (1999)
- Young Engineer Medal of Indian National Academy of Engineering (2002)
- Young Associate of the Indian Academy of Sciences (1998 – 2002)
- Fellow of the Institution of Electronics and Telecom Engineers, India
- Jagadis Bose National Science Talent Search Scholarship (1986 – 1990)

INDUSTRY AWARDS

- IESA Techno-mentor Award (2012) conferred by the Indian Electronics and Semiconductor Association
- Qualcomm Faculty Award (2021)
- IBM Faculty Award (2007)

INSTITUTE AWARDS

- Institute Silver Medal (1st rank in Btech), Computer Sc & Engg, IIT Kharagpur (1990)
- Institute Silver Medal (1st rank in MTech), Computer Sc & Engg, IIT Kharagpur (1992)
- A K Singh Distinguished Chair Professor in Artificial Intelligence, IIT Kharagpur (2018-20)

EDUCATION

1995 Ph.D. Computer Science & Engineering, Indian Institute of Technology Kharagpur.

1992 M.Tech Computer Science & Engineering, Indian Institute of Technology Kharagpur.
-- ranked first in the department with GPA of 9.6 / 10.0

1990 B.Tech Computer Science & Engineering, Indian Institute of Technology Kharagpur.
-- ranked first in the department with GPA of 9.98 / 10.0

RESEARCH PROFILE

- ~230 research publications (94 Jour,138 Conf), 23 PhD guidance, 2 US patents
- Publications grouped by areas can be found in this document. For grouping by year, please see: https://cse.iitkgp.ac.in/~pallab/publication_year.html
- Industry sponsored research (spanning 25 years) – Intel, Synopsys, SRC, National Semiconductors, Freescale Semiconductors, Texas Instruments, General Motors, IBM, Qualcomm, Google, Indian Railways, Hindustan Aeronautics Ltd.
- Areas of Research Contributions:
  - Verification Technologies for Integrated Circuits and Systems
    - Formal Verification – Assertion languages and formalisms, Model checking, Consistency and Coverage, Cohesive formal + simulation-based verification, Counter-example ranking, Formal bug taxonomies. Property grouping, Assertion refinement, Assertion-guided simulation, Assertion hierarchy for large integrated circuits, Assertion-guided fault simulation.
    - Verification of Power Intent – Formal verification of on-chip power management logic, SAT based power / timing analysis, Verification of architectural power / thermal intent.
    - Verification of Analog / Mixed-Signal Designs – AMS assertion languages and tools, Lifting assertions to real valued Features, Precision and sampling issues for assertion checking over AMS simulation, Verification of power management with analog power domains, AMS coverage management.
  - Verification of Automated Control and Embedded Systems – Control loop execution patterns with provable guarantees, SAT/SMT based verification of automated control, Energy optimization in automated control, Formal verification of railway signaling / interlocking logic, Formal verification of avionic RTOS, Formal verification of access control policies in networks
  - Verification of Intelligent Systems – Program-driven Reinforcement Learning (RL) agents in autonomous driving, Learning adaptive safety shields for safe RL, Semi-lexical languages for combining reasoning with machine learning, Mining causal relations from time series, Integrating rule-based knowledge into deep learning systems, Safety augmentation in Decision Trees, Bayesian optimization for identifying safety corners, Adversarial AI planning for finding gaps in specifications
  - Classical Artificial Intelligence – Multi-objective heuristic search, Multi-objective AND/OR Graph search, AI planning as a verification tool, Partial Order Search in Game Trees, Integrating deduction with constraint optimization, Agent searching
  - Other Areas – Computational musicology (pitch extraction from music, representing the deep structure of Indian ragas as semi-lexical languages), Distributing computing (agreement protocols, managing timing in federated automotive platforms).

TEACHING SUMMARY

- Recent Subjects – Artificial Intelligence (200+ students), Formal systems, Foundations of Computing Science, Advanced Graph Theory, Distributed Systems, Testing and Verification of Integrated Circuits
- Past Subjects – Database Management Systems, Algorithms, Operations Research, Programming and Data Structures, Computational Foundations of Cyber-Physical Systems,
- Popular lectures series in YouTube (viewed worldwide):
    - Artificial Intelligence: https://www.youtube.com/playlist?list=PL6EE0CD02910E57B8
      This series is the first AI course on NPTEL (National Program on Technology Enhanced Learning), India's national portal on technical education. This series has more than 200,000 views worldwide. An updated version of several lectures, recorded in 2020 is available here: https://www.youtube.com/playlist?list=PLLqQtEFbc-k0w19vZmFbn4SQ407CQeCwO
    - Distributed Computing: This series has more than 90,000 views worldwide. https://youtube.com/playlist?list=PLUJ7JmcrTifBROWODSG8wgyl20XgBuE-N
    - Verification: This series has been used in several companies for training. https://youtube.com/playlist?list=PLUJ7JmcrTifAatybgmAs6zc4q4m96X08G

PROFESSIONAL AND LEADERSHIP SERVICES

- Associate Editor, IEEE Trans. on Computer Aided Design of Int. Circuits and Systems (2015-2018)
- Vice Chair (India) of IEEE Council on Electronic Design Automation (2016-2018)
- Founder of Synopsys CAD Lab, IIT Kharagpur with Dr Pradip Dutta, President, Synopsys India (2009)
- Chairman, Advanced VLSI Consortium (consortium of 15 semiconductor and EDA companies) 2007-2010. This was the largest research consortium of semiconductor companies in the country at a time when the VLSI industry in India was growing in research.
- Founder of the Indo-German Center for Intelligent Transportation System in collaboration with Technical University of Munich, Germany.
- Convener of Sectional Committee on Computer Science and IT at the Indian National Academy of Engineering. (This body is responsible for shortlisting nominations for Fellows of the National Academy)
- Member of Program Advisory Committee for Core Research Grants, DST, Ministry of Science and Technology, Govt. of India (This is the grants committee for core research grants from the ministry).
- Founder and PI of FMSAFE: Center for Formal Methods in Safety Critical Systems in partnership with two other IITs. This center has been created under the IMPRINT program of India.
- Founder of the Academy of Classical and Folk Arts, IIT Kharagpur (2020 -)
- Co-Founder and Co-PI of Center for Artificial Intelligence for Societal Needs, IIT Kharagpur
- Co-Founder and Co-Principal Investigator of Science and Heritage Initiative (SandHI), IIT Kharagpur
- Co-Founder and Co-Principal Investigator of General Motors Collaborative Research Lab, IIT Kharagpur
- Professor-in-charge of SPIC MACAY, IIT Kharagpur Chapter (2000 – 2016)
- Co-Founder of Advanced Manufacturing Consortium, IIT Kharagpur (conceived the consortium model as the Dean, Sponsored Research and Industrial Consultancy, IIT Kharagpur).
- Council Member of Indian Association for Research in Computer Science (2013-2014)

FORAYS IN MUSIC AND CULTURE

I play an Indian Classical stringed instrument called the sitar (shown in the picture).

I am currently collaborating with Padma Bhushan Pt Ajoy Chakraborty, legendary classical vocalist and scholar, on studying the deep structure of Indian Ragas and their representation as semi-lexical languages – a study which is expected to highlight the creative liberty in Indian Classical Music from a cognitive perspective.

I am also using the raga system to understand the cohesion between imitation based learning and grammar (rule) based learning, and translating that to combinations of rule-based reasoning and machine learning.

PhD THESIS GUIDANCE

Awarded:

1. Design Intent Verification by Formal Property Coverage, *Prasenjit Basu.*
2. Formal Analysis of Property Specifications: Consistency, Coverage and Synthesis, *Sayantan Das*
3. Formal Methods for accelerating formal, semi-formal and dynamic property verification through novel specification styles, *Ansuman Banerjee*
4. SAT Based Solutions for Timing and Power Estimation in Gate Level Circuits, *Suchismita Roy*
5. Formal and semi-formal verification methods with constrained random test benches, *Bhaskar Pal*
6. A symbolic event propagation approach for solving timing problems of digital circuits, *Arijit Mondal*
7. Model checking techniques for Reasoning about Events and Extremal Properties in Timed Systems, *Jatindra Kumar Deka*
8. Formal Methods for Early Time-Budgeting in Component-based Embedded Control Systems, *Manoj Dixit*
9. Formal Analysis of Security Policy Implementations in Enterprise Networks, *Padmalochan Bera*
10. Assertions – from a mixed-signal perspective, *Subhankar Mukherjee*
11. Formal and Semi-Formal Methods for Application Specific Usage Control and Security, *Rajkumar P.V.*
12. Formal Methods for Aiding Verification of Local Design Changes in Digital Integrated Circuits, *Srobona Mitra* [Winner of Google Women in Engineering Award]
13. Search Techniques for finding Alternative Solutions for AND/OR Graphs and Bi-objective Optimization Problems, *Priyankar Ghosh*
14. Formal Methods for Architectural Power Intent Verification and Functional Reliability Analysis, *Aritra Hazra* [Winner of ACM India Best PhD Dissertation, IBM Best PhD thesis, IESA Technovation Award]
15. Automated Planning Based Methods for Early Verification of Reactive Control Systems, *Kamalesh Ghosh*
16. Assertion Based Analysis of Mixed Signal Systems, *Antara Ain*
17. Multi-rate Strategies for Power and Bandwidth Optimization in Embedded Control, *Rajorshee Raha*
18. A Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems, *Sumana Ghosh*
19. Algorithms for Formal Feature Analysis and Inference Learning for Hybrid Systems, *Antonio A Bruto da Costa*
20. Revisiting Fault-Analysis of Block Ciphers: Attacks, Defenses and Evaluation Frameworks, *Sayandeep Saha*
21. A Unified Framework for Pitch Extraction from Human Voice, *Pradeep Rengaswamy*
22. Hierarchical Planning and Control in Model-based Design of Systems and Circuits, *Rajib Lochan Jana*
23. Management and Verification of Power and Thermal Contracts in Integrated Circuits, *Sudipa Mandal*

SPONSORED RESEARCH

A. SELECTED INDUSTRY SPONSORED PROJECTS

Domain: Verification of Digital Integrated VLSI Circuits

1 **Intel** (Folsom, USA and Haifa, Israel) 2002 - 2005
Formal methods for verification of architectural properties and computing formal coverage metrics was integrated into Intel's Formal Verification tool suite developed at Intel, Haifa.

2 **National Semiconductors**, (Santa Clara, USA) 2003 – 2007
A tool called GENSTIMULI was developed for the Technology Infrastructure Group of National Semiconductors (now TI), which uses formal methods for generating tests for custom cell characterization.

3 **Synopsys** (Bangalore, India and Massachusetts, USA) 2000 – 2008
Design of Assertion Languages and Formal Specification Formalisms (some of which are now part of the SystemVerilog Standards). Several toolkits and patented verification technologies were developed.

4 **Intel** (Bangalore, India) 2009 – 2012
Formal methods for post-silicon validation of bug-fixes and Counter-example Ranking in Intel's processors. PhD student, Srobona Mitra, won the Google Anita Borg Woman in Engineering Award for this work.

5 **Synopsys CAD Laboratory** 2009 –
Synopsys CAD Labs, IIT Kharagpur was set up for undertaking projects in the areas of design automation for verification, testing, and security. Synopsys conferred the prestigious Charles Babbage Grant to this Lab.

Domain: Verification of Mixed-Signal Integrated Circuits

1 **National Semiconductor** Corp., (Greenock, Scotland) 2007 – 2010
Methods for verifying integrated power management units (PMUs) which are large integrated AMS circuits used in portable power devices like cell phones, PDAs and Laptops. The methods use formal hybrid automata based behavioral models.

2 **Semiconductor Research Corporation** (SRC), USA 2008 – Date
Technology for verification of formal analog properties over AMS simulators. Phase-2 of the project deals with abstract interpretation of formal equivalence features between AMS designs/models.

3 **Texas Instruments** (custom funded via Semiconductor Research Corp) 2018 – Date
Technology for formal coverage management of large analog and mixed-signal integrated circuits.

4 **Intel**, USA 2018 – 2021
Technology for mining dense time assertions from time series data

Domain: Verification of Power Intent and Power Management Strategies

1 **Synopsys** (California, USA and Bangalore, India) 2008 – 2013
Formal verification technology for verifying the architectural power management strategy of large integrated circuits. A tool has been developed using the technology.

2 **Intel** (Bangalore, India) 2010 – 2012
Tool for evaluating power management strategies for mobile portable platforms.

3 **Intel** Global Research (USA) 2015- Date
Formal verification of power management strategies for mixed-signal power domains.

Domain: Verification of Automotive Control

1 **General Motors** (India Science Labs) 2007 – 2009
Technology for verification of formal properties on the fly over execution traces of UML state-charts was integrated into a tool being used by GM for verification of automotive control software.

2 **General Motors** (India and Warren, USA) 2009 – 2012
Formal verification of feature specifications for automotive control subsystems using AI planning techniques. This research led to a joint patent with General Motors.

Domain: Software Verification

1 **Google**. 2008 – 2009
Developing formal methods for verifying web-service protocols

2 **Hindustan Aeronautics Ltd.** 2015 – 2018
Formal verification of India's first indigenous avionic Real Time Operating System. The RTOS is now flying with the Hawkeye aircraft of HAL.

Domain: Verification of Railway Signaling and Interlocking

1 **Indian Railways** 2013 -- 2017
Formal methods for proving the correctness of Electronic Interlocking Logic for railway signaling.

B. SELECTED GOVERNMENT SPONSORED PROJECTS

1 **Developing Explainable Artificial Intelligence for Connected and Autonomous Vehicles** (2019-2021)
DST-UKIERI project in collaboration with the Warwick Manufacturing Group, UK. This project aims to develop explainable and safe reinforcement learning frameworks for autonomous driving and ADAS tasks.

2 **Artificial Intelligence For Societal Needs** (2013-2017)
This project funded under the Diamond Jubilee Research Grant, IIT Kharagpur brought together researchers from various departments to work for AI solutions to problems in Agriculture, Environment, Power, Disaster Management and Urban Planning.

3 **FMSAFE: A Networked Centre for Formal Methods for Safety Critical Systems** (2017-2020)
This IMPRINT project funded by MHRD and Ministry of Railways, brings together experts from IIT Kharagpur, IIT Bombay and IIT Kanpur to develop formal verification technology for safety critical systems.

4 **Decoding And Exploring Ancient Classification of Ragas In Indian Classical Music (**2014-2018)
This project was funded by MHRD under the Science and Heritage Initiative (SandHI). Collaboration with Indian Classical musicians in studying the deep structure of Indian Ragas.

5 **AUTOSAFE: Architecture- Aware Timing Analysis And Formal Verification of Automotive Control Systems** (2012-2015)
This project was funded by the Indo-German Science and Technology Center to IIT Kharagpur and TU Munich. This project laid the foundations for the two universities to come together to set up an Indo-German Center for Intelligent Transportation Systems at IIT Kharagpur recently.

TOOLS AND TECHNOLOGY

PATENTS

US PATENT No: US 7,797,123 Sep 14, 2010

- ***Method and Apparatus for Extracting Assume Properties from a Constrained Random Test Bench***, Inventors: K.Dey, E.Cerny, Pallab Dasgupta, B.Pal, P.P.Chakrabarti.

This patent describes a technique for automatically extracting formal logical constraints on the environment of a circuit, where the environment is described by means of a test-bench developed in SystemVerilog. Developing environment constraints (called *assume properties*) is a non-trivial task and is one of the main concerns in formal verification of reactive systems. The patented technique automated this problem. The patent was jointly obtained with collaborators from Synopsys Inc, and is assigned to Synopsys.

US PATENT No: US 8,082,140, Dec 20, 2011

- ***Parametric Analysis of Real Time Response Guarantees on Interacting Software Components***, Inventors: M.Dixit, S.Ramesh, Pallab Dasgupta.

This patent describes a technique for automatic extraction of linear constraints on the timing of constraint behaviors that are obtained by formally comparing the conjunction of component specifications with formal time-critical end-to-end behaviors in automotive features. The patented technique enables early timing analysis with the help of formal specifications in the development of automotive control features and sub-system technical specifications. The patent was jointly obtained with collaborators from General Motors, and is assigned to General Motors.

TOOLS DEVELOPED AND MAINTAINED BY THE RESEARCH GROUP

PSI-MINER

This is a first of its kind tool for finding temporal causal relations for explaining events in time series data. Developed under a Intel CAD-SRS research grant, this tool is available in the public domain: https://github.com/antoniobruto/PSIMiner

SaVerECS

This is a SMT-based verification tool to formally guarantee the performance and safety of an embedded control software under the influence of process or measurement noises and timing uncertainties (delay, jitters), before implementing them in real-time systems. Support for *non-linearities in the controlled plant and the controller software*, *real-valued constraints* and *control software code as input*, make this tool-chain ideal for verifying real-world hybrid systems. Our tool incorporates semantic support for capturing plant specifications, timing and value-based uncertainties (noise, precision errors), and the control software code. https://github.com/saverecs/SaverECS

CHAMS, DYFET AND FORFET: AMS ASSERTION AND FEATURE EVALUATION TOOLS

This tool suite enables any standard AMS circuit simulator to monitor analog time domain properties and features. These were developed under a recent project sponsored by the Semiconductor Research Corporation (SRC) which is a consortium of semiconductor and EDA companies. One version of this tool has been adopted by Freescale Semiconductors (now NXP). The ForFET tool is now available in the public domain: https://github.com/antoniobruto/ForFET

CoverT

This tool has been developed for Texas Instruments under a research contract from Semiconductor Research Corporation. This is a coverage management tool for large analog and mixed signal integrated circuits. The tool has been integrated into TI's verification environment.

CHASSIS

Verification tool for integrated power management chips. This tool was developed under a collaboration with National Semiconductor Corp, UK for verifying integrated PMUs, which are large scale analog-mixed circuits consisting of linear drop-out regulators, buck regulators and battery chargers. The tool introduced the use of behavioral models based on hybrid automata into the design validation flow of National semiconductors.

POWER-TRUCTOR

Formal verification tool for verifying the architectural power management strategy in large digital integrated circuits. This tool has been developed under the Synopsys CAD Laboratory at IIT Kharagpur.

RAILTOOLS FOR SIGNALING VALIDATION

This tool suite proves the correctness of signaling logic developed for electronic signaling and interlocking systems using formal methods. The tool has been tested on several railway yards in India and is now being considered by RDSO for widespread adoption in the Indian Railways.

PAST TOOLS – NOT MAINTAINED ANYMORE

GEN-STIMULI

This tool was developed for generating minimum length stimulus patterns for custom cell characterization. Adopted by National Semiconductors, this tool uses formal state space analysis to find the shortest stimuli for characterization tests like setup and hold.

COV-ANALYZER

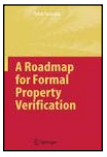
Formal verification coverage analysis tool. This tool has been integrated with the Forspec/Forecast tool suite of Intel with collaboration with the electronic design automation group at Intel, Haifa. The development of this tool was sponsored by the chipset design group at Intel, Folsom, USA.

SPEC-MATCHER

Formal design intent verification tool for digital integrated circuits. This tool was also developed under the research collaboration with Intel. These contributions have been noted in the article, *Fifteen Years of Formal Property Verification at Intel* by Dr Limor Fix, Director, Intel Research Lab, Pittsburgh, in the book, *25 Years of Model Checking*, Springer, 2008, ISBN: 978-3-540-69849-4.

PUBLICATIONS

BOOKS



A Roadmap for Formal Property Verification.
Pallab Dasgupta**,** Springer, 2006.

Multi-objective Heuristic Search.
Pallab Dasgupta**,** P.P. Chakrabarti, S.C. DeSarkar,
Vieweg Verlag, Germany, 1999.

Cohesive Coverage Management Leveraging Formal Test Plans
Artitra Hazra, Pallab Dasgupta, P.P. Chakrabarti, Lambert Academic Publishing, 2012

BOOK CHAPTERS

	Book Chapters	Authors	Publisher, Year
1	*Can Semi-Formal be made more Formal?* Book Title: *Next Generation Design and Verification Methodologies for Distributed Embedded Control Systems.* Ed: S.Ramesh, P.Sampath.	Ansuman Banerjee, Pallab Dasgupta, P.P. Chakrabarti	Springer, 2007
2	*Agent Searching.* Book Title: *Computational Mathematics, Modelling and Algorithms*	Pallab Dasgupta**,** P.P. Chakrabarti, S.C.DeSarkar	Narosa Publishing House, 1999
3	*Early Time Budgeting for Component-Based Embedded Control Systems.* Book Title: *Embedded Systems Development* Ed: A. S-Vincentelli, H. Zeng, M.Di-Natale, P.Marwedel	Manoj J Dixit, S. Ramesh, Pallab Dasgupta	Springer, 2014
4	*Formal Assurance of Signaling Safety: A Railways Perspective.* Book Title: *Handbook of Research on Emerging Innovations in Rail Transportation Engineering* Ed: B Umesh Rai	Pallab Dasgupta Mahesh Mangal	IGI Global, May 2016
5	*A Logical Perspective of Formal Verification: A Narrative on the Genesis and Evolution of the Formal Verification Group at IIT Kharagpur* Book Title: *The Mind of an Engineer* Ed: Purnendu Ghosh, Baldev Raj, INAE	Pallab Dasgupta	Springer 2016
6	*On the Deep Structure of Ragas and Analytic Rating of Music Scores* Book Title: *Heritage Preservation – A computational approach* Ed: Bhabatosh Chanda, Subhasis Chaudhuri, Santanu Chaudhury	Sudipa Mandal, Shilpi Chaudhuri, Antonio Anastasio Bruto da Costa, Gouri Karambelkar, Pallab Dasgupta	Springer 2018

JOURNAL PUBLICATIONS (GROUPED BY AREA)

ARTIFICIAL INTELLIGENCE

J1. Sumanta Dey, Anusha Mujumdar, Pallab Dasgupta, Soumyajit Dey, Adaptive Safety Shields for Reinforcement Learning-based Cell Shaping. ***IEEE Transactions on Networks and Service Management***, 2022, DOI: 10.1109/TNSM.2022.3194566.

J2. Briti Gangopadhyay, Pallab Dasgupta, and Soumyajit Dey, Safe and Stable RL (S2RL) Driving Policies Using Control Barrier and Control Lyapunov Functions. ***IEEE Transactions on Intelligent Vehicles***, 2022, doi: 10.1109/TIV.2022.3160202.

J3. Briti Gangopadhyay; Somnath Hazra; Pallab Dasgupta, Semi-Lexical Languages: A Formal Basis for using Domain Knowledge to Resolve Ambiguities in Deep-Learning based Computer Vision, ***Pattern Recognition Letters***, 152, 143-149, 2021.

J4. Briti Gangopadhyay, Harshit Soora, Pallab Dasgupta, Hierarchical Program-Triggered Reinforcement Learning Agents For Automated Driving, ***IEEE Trans. on Intelligent Transportation Systems***, DOI: 10.1109/TITS.2021.3096998, (2021).

J5. Antonio Anastasio Bruto da Costa, Pallab Dasgupta, Learning Temporal Causal Sequence Relationships from Real-Time Time-Series, ***Journal of Artificial Intelligence Research*** (JAIR), 70: 205-243 (2021).

J6. Kamalesh Ghosh, Pallab Dasgupta and S. Ramesh, Automated Planning as an Early Verification Tool for Distributed Control, ***Journal of Automated Reasoning***, 54 (1), 31-68, 2015.

J7. Subhankar Mukherjee, P. Dasgupta, A Fuzzy Real Time Temporal Logic*, Int. J. Approx. Reasoning*, 54(9): 1452-1470, 2013.

J8. Priyankar Ghosh, Amit Sharma, P. P. Chakrabarti, Pallab Dasgupta: Algorithms for Generating Ordered Solutions for Explicit AND/OR Structures. ***Journal of Artificial Intelligence Research***, (JAIR) 44: 275-333 (2012)

J9. M. Dixit, S.Ramesh and P. Dasgupta. Some results on Parametric Temporal Logic. *Information Processing Letters,* 111(20): 994-998, 2011.

J10. A. Banerjee and P. Dasgupta. The Open Family of Temporal Logics: Annotating Temporal Operators with Input Constraints. ***ACM Transactions on Design Automation and Embedded Systems*** *(TODAES),* 10 (3), 492-522, 2005.

J11. K. Chatterjee, P. Dasgupta, P.P. Chakrabarti. The power of first-order quantification over states in branching and linear time temporal logics. *Information Processing Letters,* 91: 201-210, 2004.

J12. K. Chatterjee, P. Dasgupta, P.P. Chakrabarti. A branching time temporal framework for Quantitative Reasoning. ***Journal of Automated Reasoning,*** 30: 205-232, 2003.

J13. P.Dasgupta, P.P.Chakrabarti, Arnab Dey, S.Ghose and W.Bibel. Solving constraint optimization problems from CLP-style specifications using heuristic search techniques. ***IEEE Transactions in Knowledge and Data Engineering,*** 14 (2), 2002, 353-368.

J14. P. Dasgupta, P.P.Chakrabarti, J.K. Deka. Min-max event triggered computation tree logic. *Sadhana, (Spl. Issue on Formal Verification),* 27 (2): 163-180, 2002.

J15. A.C.Patthak, I.Bhattacharya, A.Dasgupta, P.Dasgupta, P.P.Chakrabarti. Quantified Computation Tree Logic. *Information Processing Letters,* 82(3): 123-129, 2002.

J16. P.Dasgupta, Jatindra K. Deka, P.P.Chakrabarti and S. Sriram. Min-max Computation Tree Logic. ***Artificial Intelligence***, 127 (2001), 137-162.

J17. P.Dasgupta, Jatindra K. Deka and P.P.Chakrabarti. Model checking on Timed Event Structures. ***IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems***, Vol 19, No 5, May 2000, 601-611.

J18. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. Multiobjective Heuristic Search of AND/OR Graphs. ***Journal of Algorithms***, 20 (1996) 282-311.

J19. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. Searching Game Trees under a Partial Order. ***Artificial Intelligence***, 82 (1996) 237-257.

J20. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. Agent Searching in Uniform *b-ary* Trees: Multiple Goals and Unequal Costs. *Information Processing Letters*, 58 (1996) 311-318.

J21. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. New results on Multiobjective State Space Search. *Sadhana*, 21, 3 (1996), 263-290.

J22. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. Utility of *Pathmax* in Partial Order Heuristic Search. *Information Processing Letters*, 55 (1995) 317-322.

J23. P.Dasgupta, P.P.Chakrabarti, S.C.DeSarkar. A correction to Agent Searching in a tree and the optimality of Iterative Deepening. *Artificial Intelligence*, 77 (1995) 173-176.

J24. P.Dasgupta, P.P.Chakrabarti and S.C.DeSarkar. Agent Searching in a tree and the optimality of Iterative Deepening. ***Artificial Intelligence***, 71 (1994) 195-208.

ANALOG / MIXED-SIGNAL CAD FOR VERIFICATION

J25. S. Sanyal Pallab Dasgupta, et al., The CoveRT Approach for Coverage Management in Analog and Mixed Signal Integrated Circuits, ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, doi: 10.1109/TCAD.2022.3157686.

J26. Sudipa Mandal, Pallab Dasgupta. Migrating Assertions from Dense to Discrete Time, ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, doi: 10.1109/TCAD.2021.3101715.

J27. Sayandeep Sanyal, Antonio Anastasio Bruto da Costa, Pallab Dasgupta. Recurrence in Dense-time AMS Assertions, ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, 40(11), 2416-2420 (2021).

J28. Sayandeep Sanyal, Mayukh Bhattacharya, Amit Patra, Pallab Dasgupta, A Methodology for Identification of Internal Nets for Improving Fault Coverage in Analog and Mixed Signal Circuits, *Journal of Electronic Testing: Theory and Applications*, Springer, 36(6): 719-730 (2020).

J29. Antara Ain, Pallab Dasgupta, Interpreting Local Variables in AMS Assertions during Simulation, ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, 38(5): 980-984 (2019).

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